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| 10/090,371 | 03/04/2002 | Dawei Huang | HUANG 2-1 (58655) | 5175 |

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WILLIAMS, MORGAN & AMERSON/LUCENT
10333 RICHMOND, SUITE 1100
HOUSTON, TX 77042

| EXAMINER | |
|---|---|
| TORRES, JOSEPH D | |
| **ART UNIT** | **PAPER NUMBER** |
| 2133 | |

DATE MAILED: 05/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/090,371 | HUANG ET AL. | |
| | Examiner | Art Unit | |
| | Joseph D. Torres | 2133 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *04 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.



9-6-0.

## DETAILED ACTION

### *Response to Arguments*

1. Applicant's arguments with respect to claims 1-22 have been considered but are moot in view of the new ground(s) of rejection.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 17-22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 17 recites, "A method of channel coding data in a digital communications system", in the preamble and "trellis encoding the expanded digital input data sequence to produce a channel coded data stream by **producing a generator matrix having the constraint length**", in lines 9 of the body of claim 17. The Examiner asserts that nowhere in the specification does the Applicant teach "producing a generator matrix having the constraint length" as part of a "method of channel coding data in a digital communications system" or as part of "trellis encoding the expanded digital input data sequence to produce a channel coded data stream".

The Applicant instead teaches that the "method of channel coding data in a digital communications system" and for "trellis encoding the expanded digital input data sequence to produce a channel coded data stream" is performed by the receiving circuit 12 and convolutional encoder 14 in the Applicant's Figure 1, whereby the encoding of received digital input data is based on a generating matrix, but nowhere does the Applicant teach that the trellis encoding device produces a generating matrix.

Note: Figure 5 is presumably the generating matrix upon which receiving circuit 12 and convolutional encoder 14 are designed, but nowhere does the Applicant teach that the receiving circuit 12 and convolutional encoder 14 produce the generating matrix of Figure 5.

Claim 3 recites, "the inserted zeros comprise an equivalent time varying convolutional code". Nowhere in the application does the Applicant teach "inserted zeros comprise an equivalent time varying convolutional code".

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In line 5 of claim 1, "based on" is indefinite since it is not clear how "constraint length" is used for forming an expanded digital input data sequence.

In line 9 of claim 1, "according to" is indefinite since it is not clear how "constraint length" is used for by "said encoder".

Claim 3 recites, "the inserted zeros comprise an equivalent time varying convolutional code", which is nonsense since zeros are zeros not a convolutional code.

In line 5 of claim 10, "based on" is indefinite since it is not clear how "constraint length" is used for forming an expanded digital input data sequence.

In line 6 of claim 10, "based on" is indefinite since it is not clear how "constraint length" is used for forming an expanded digital input data sequence.

Claim 12 recites, "the inserted zeros comprise an equivalent time varying convolutional code", which is nonsense since zeros are zeros not a convolutional code.

In line 5 of claim 17, "based on" is indefinite since it is not clear how "constraint length" is used for forming an expanded digital input data sequence.

Claim 19 recites, "the inserted zeros comprise an equivalent time varying convolutional code", which is nonsense since zeros are zeros not a convolutional code.

Claims 1-22 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

Claim 1 recites, "forming an expanded digital input data sequence based on a constraint length". The omitted structural cooperative relationships are: the relationship between "forming an expanded digital input data sequence" and "constraint length".

Claim 1 recites, "said encoder operative according to the constraint length". The omitted structural cooperative relationships are: the relationship between "said encoder" and "constraint length".

Claim 3 recites, "the inserted zeros comprise an equivalent time varying convolutional code". The omitted structural cooperative relationships are: the relationship between "the inserted zeros" and "an equivalent time varying convolutional code".

Claim 10 recites, "forming an expanded digital input data sequence based on a constraint length". The omitted structural cooperative relationships are: the relationship between "forming an expanded digital input data sequence" and "constraint length".

Claim 10 recites, "trellis encoding the expanded digital input data sequence based on a constraint length". The omitted structural cooperative relationships are: the relationship between "trellis encoding the expanded digital input data sequence" and "constraint length".

Claim 12 recites, "the inserted zeros comprise an equivalent time varying convolutional code". The omitted structural cooperative relationships are: the relationship between "the inserted zeros" and "an equivalent time varying convolutional code".

Claim 17 recites, "forming an expanded digital input data sequence based on a constraint length". The omitted structural cooperative relationships are: the relationship between "forming an expanded digital input data sequence" and "constraint length".

Claim 19 recites, "the inserted zeros comprise an equivalent time varying convolutional code". The omitted structural cooperative relationships are: the relationship between "the inserted zeros" and "an equivalent time varying convolutional code".

### *Claim Rejections - 35 USC § 101*

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 10-22 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The body of claims 10-22 comprises an abstract algorithm that can be carried out by hand or in computer program. Abstract algorithms are non-statutory. Computer programs are non-statutory.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Simanapalli; Sivanand (US 6081921 A) in view of Kato; Osamu et al. (US 5436918 A, hereafter referred to as Kato).

35 U.S.C. 103(a) rejection of claims 1, 4 and 10.

Simanapalli teaches a data receiving circuit for receiving a digital input data sequence and periodically inserting known symbols into the digital input data sequence and forming an expanded digital input data sequence based on a constraint length (Bit Insertion Controller 28, Zero Bit Input Source 24 and Register 26 in Figure 2 of Simanapalli is a data receiving circuit for receiving a digital input data sequence 18 comprising Zero Bit Input Source 24 for periodically inserting known symbols into the digital input data sequence and forming an expanded digital input data sequence stored in register 26 based on a constraint length of 2; Note: the Merriam-Webster Collegiate Dictionary defines constrain as to force by imposed stricture, restriction or limitation and constraint as the act of constraining; since bit insertion is limited or restricted to being periodically inserted after every input bit the constraint length for periodic insertion used for forming the expanded digital input data sequence is 2); and an encoder operatively connected to said data receiving circuit for trellis encoding the expanded digital input data sequence to produce a channel coded data stream such that the number of connections between trellis nodes in a trellis **can be** reduced (Logic Circuit 30 is an encoder operatively connected to said data receiving circuit for trellis encoding the expanded digital input data sequence to produce a channel coded data stream such

that the number of connections between trellis nodes in a trellis **can be** reduced), said encoder operative according to a constraint length.

However Simanapalli does not explicitly teach the specific use of the number of connections between trellis nodes in a trellis are reduced.

Kato, in an analogous art, teaches use of the number of connections between trellis nodes in a trellis are reduced (Kato teaches that since an inserted bit is known at the decoder in Figure 4B of Kato connections to the nodes for inserted bits in the Trellis of Figure 7 in Kato are known which reduces connections by not having to connect to any of the other nodes for the inserted bit, see Figure 3 in Kato for comparison).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Simanapalli with the teachings of Kato by including use of the number of connections between trellis nodes in a trellis are reduced. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of the number of connections between trellis nodes in a trellis are reduced would have provided the opportunity to reduce calculation over the trellis during decoding of a convolutional code.

35 U.S.C. 103(a) rejection of claims 2, 3, 11 and 12.

The Abstract in Kato teaches that the inserted bit can be a one or a zero.

35 U.S.C. 103(a) rejection of claims 5 and 13.

Convolutionally coded codewords are inherently in a one-to-one mapping with the distinct paths on a trellis to binary sequences.

35 U.S.C. 103(a) rejection of claims 6 and 14.

Note: the encoder of Figure 4A in Kato is inherently capable of inserting bits into any position of the received data stream. See In re Swinehart, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971) and In re Schreiber, 128 F.3d 1473, 1477, 44 USPQ2d 1429, 1431 (Fed. Cir. 1997).

35 U.S.C. 103(a) rejection of claim 7.

Convolutionally coded codewords are inherently operative as a generator matrix having a constraint length k=m-1, wherein m corresponds to the memory length, and the code rate is R=1/l. Note: the encoder of Figure 4A in Kato is inherently capable of inserting bits into any position of the received data stream. See In re Swinehart, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971) and In re Schreiber, 128 F.3d 1473, 1477, 44 USPQ2d 1429, 1431 (Fed. Cir. 1997).

In addition, col. 1, lines 15-51 of Simanapalli teach a k'/n convolutional encoder with constraint length N so that if n=l and k'=1, then the k'/n convolutional encoder is a 1/l convolutional encoder with code rate 1/l and if N=2 then zero bits are inserted every N-1 information bits. That is, the teaching in Simanapalli encompass a code rate 1/l whereby o bits are inserted every N-1 information bits.

35 U.S.C. 103(a) rejection of claims 8, 9, 15 and 16.

Col. 1, lines 25-31 in Kato teach a Maximum Likelihood (ML) decoder comprising a Viterbi decoder.

35 U.S.C. 103(a) rejection of claim 17.

Simanapalli teaches a data receiving circuit for receiving a digital input data sequence and periodically inserting known symbols into the digital input data sequence and forming an expanded digital input data sequence based on a constraint length (Bit Insertion Controller 28, Zero Bit Input Source 24 and Register 26 in Figure 2 of Simanapalli is a data receiving circuit for receiving a digital input data sequence 18 comprising Zero Bit Input Source 24 for periodically inserting known symbols into the digital input data sequence and forming an expanded digital input data sequence stored in register 26 based on a constraint length of 2; Note: the Merriam-Webster Collegiate Dictionary defines constrain as to force by imposed stricture, restriction or limitation and constraint as the act of constraining; since bit insertion is limited or restricted to being periodically inserted after every input bit the constraint length for periodic insertion used for forming the expanded digital input data sequence is 2); and an encoder operatively connected to said data receiving circuit for trellis encoding the expanded digital input data sequence to produce a channel coded data stream such that the number of connections between trellis nodes in a trellis **can be** reduced (Logic Circuit 30 is an encoder operatively connected to said data receiving circuit for trellis encoding the expanded digital input data sequence to produce a channel coded data stream such

that the number of connections between trellis nodes in a trellis **can be** reduced), said encoder operative according to a constraint length.

However Simanapalli does not explicitly teach the specific use of the number of connections between trellis nodes in a trellis are reduced.

In addition, col. 1, lines 15-51 of Simanapalli teach a k'/n convolutional encoder with constraint length N so that if n=l and k'=1, then the k'/n convolutional encoder is a 1/l convolutional encoder with code rate 1/l and if N=2 then zero bits are inserted every N-1 information bits. That is, the teaching in Simanapalli encompass a code rate 1/l whereby o bits are inserted every N-1 information bits.

Kato, in an analogous art, teaches use of the number of connections between trellis nodes in a trellis are reduced (Kato teaches that since an inserted bit is known at the decoder in Figure 4B of Kato connections to the nodes for inserted bits in the Trellis of Figure 7 in Kato are known which reduces connections by not having to connect to any of the other nodes for the inserted bit, see Figure 3 in Kato for comparison).

In addition, col. 1, lines 15-51 of Kato teach a ½ convolutional encoder with constraint k=3 so that if l=2, then the ½ convolutional encoder is a 1/l convolutional encoder with code rate 1/l.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Simanapalli with the teachings of Kato by including use of the number of connections between trellis nodes in a trellis are reduced. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that

use of the number of connections between trellis nodes in a trellis are reduced would have provided the opportunity to reduce calculation over the trellis during decoding of a convolutional code.

35 U.S.C. 103(a) rejection of claims 18 and 19.

The Abstract in Kato teaches that the inserted bit can be a one or a zero.

35 U.S.C. 103(a) rejection of claim 20.

Convolutionally coded codewords are inherently in a one-to-one mapping with the distinct paths on a trellis to binary sequences.

35 U.S.C. 103(a) rejection of claims 21 and 22.

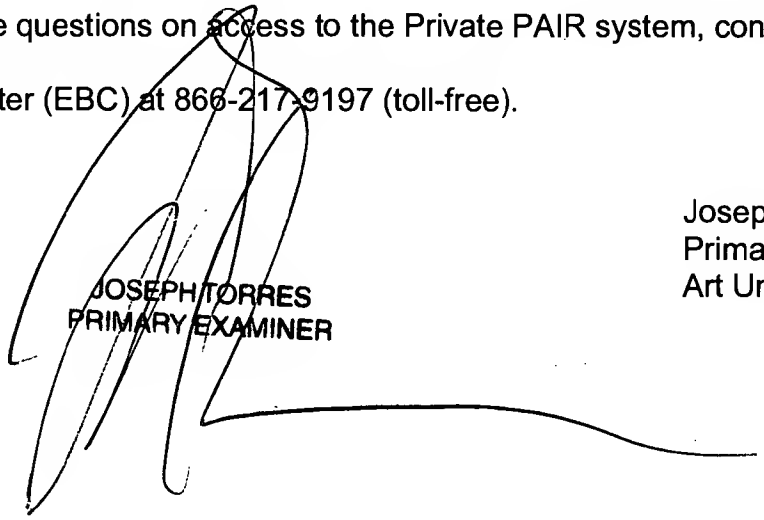
Col. 1, lines 25-31 in Kato teach a Maximum Likelihood (ML) decoder comprising a Viterbi decoder.

***Conclusion***

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).




Joseph D. Torres, PhD
Primary Examiner
Art Unit 2133